# Mark C. Lee

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Seeking an interesting and challenging position in an innovative company that leverages my technical and leadership skills.

## Expertise

**12 years of RTL-to-GDSII ASIC design flow expertise**

- Delivery of design flows for server CPUs, discrete GPUs, and next-generation Fusion client processors
- Continuous delivery under intense schedule demands using bleeding edge process technology to deliver on extreme performance, area, and power requirements
- Knowledgeable of EDA industry capabilities/limitations and the ability to drive and build innovative internal solutions when necessary

**8 years of people and technical leadership**

- Leading multiple initiatives spanning groups and business units
- Leading a team of 70+ across North America and Asia
- Continuously high technical and management ratings with emphasis on team-building and mentoring
- Nominated to AMD's Experienced Managers Academy 2008, Director's Leadership Experience 2010

## Education

***Massachusetts Institute of Technology*** – Cambridge, MA

1998 Master's of Engineering in Electrical Engineering and Computer Science
1997 Bachelor's of Science in Electrical Engineering

## Experience

4/00 - ***AMD Inc.*** ***(Formerly ATI Technologies Inc.)*** **– Graphics Silicon Engineering** – Sunnyvale, CA

7/09- **Design Methodology and Physical Design Director**

Lead the SOC & IP Design Methodology and CAD Team to deliver a flexible design flow for server, fusion CPUs, discrete GPUs, and South Bridge chips. In addition, lead the Sunnyvale Physical Design Team in executing AMD Radeon's enthusiast class discrete graphics chips. Responsible for 70+ team members spread across North America and Asia.

6/06-7/09 **SOC Integration Senior Manager – Design Methodology**

Lead a design methodology team spanning 5 geographic sites to deliver a chip design flow from RTL Synthesis to Physical Design. Areas of responsibility include hierarchical netlisting, chip assembly, chip floorplanning, toplevel budgeting, IP management, logical equivalence, netlist quality, full chip place-and-route and full chip timing and noise closure. Driving technical management and design specification to support project teams across multiple geographic locations simultaneously while interfacing externally with

EDA vendors to deliver on world-class design methodology.

11/04-6/06 **Physical Design Manager - Integration and Timing Closure**

Built and managed a team for Physical Integration for ATI's Radeon 3800 and 2900 series of products and Full Chip Timing Closure for the 2900 family. Physical Integration includes chip floorplanning, block sizing and pin assignments, timing budgeting, netlist quality checks, and IP integration and management. Full Chip Timing Closure challenges include constraint management, STA flow and execution, SI validation, capacity/runtime issues, and hierarchical design complications. Owned technical management, flow and schedule ownership and execution, employee training and development, and some technical duties. Chips implemented in TSMC 80um and 55nm process ranging from 600M to 700M transistors.

11/03-11/04 **Physical Design Manager – CAD**

Owned project CAD support and future CAD initiatives

11/02-11/03 **Physical Design Manager**

Managed entire Physical Design Team of 20+ engineers from gates-to-gdsii for the Radeon X800 (Pro/XT/XT-PE) product manufactured using a TSMC 0.13um process technology with 160M+ transistors. Owned technical management, project schedule ownership and execution, flow development and execution, and had some technical duties. Design space included chip and block level floorplanning, timing budgeting, placement, CTS, routing, physical optimization, and various timing and physical validation. Interfaced with foundry for tapeout and silicon validation activities, resulting in first silicon production.

4/02-11/02 **Staff Engineer**

Owned Physical Design duties for the Textures Block for the Radeon 9600 product manufactured using TSMC 0.13um process with 75M+ transistors. Executed block level floorplanning, placement, CTS, routing, physical optimization, and timing and physical validation. Owned flow development and support for hiVt cell swapping to improve leakage power throughout the chip.

4/00-4/02 **Senior Engineer**

Owned Front End Netlist Integration and Full Chip Timing for the Radeon 9700 product using TSMC 0.15um process with 110M+ transistors. Owned flow development and execution for both activities.

8/99-4/00 ***Artx, Inc.*** **- Member of Technical Staff** – Palo Alto, CA

Owned the Audio Interface (AI) for Nintendo Gamecube's GPU Flipper using NEC 0.18um process with 51M+ transistors. Using a given design spec, owned logic design and verification of the AI. Verification included block level verilog testbenches, C model, chip level verification support, and post-silicon lab work. Also owned chip level gate level simulations for Flipper. Artx was acquired by ATI in 2000.

9/98-8/99 ***SGI*** **- Member of Technical Staff, Advanced Graphics Division** – Mtn View, CA

Contributed to Raster Chip verification on the Bali Project, a next generation high end

graphics system. Duties included writing block level tests and C models.

## Misc

US Citizen, verbally fluent in Mandarin Chinese
References Available Upon Request